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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,533	01/18/2002	Michael J. Graziano	56162.000352	7745

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,533	GRAZIANO ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002 and 30 May 2002 and 24 J*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 15-17, and 19-29* is/are rejected.

7)☒ Claim(s) *14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/30/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-13, 15-17, and 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Allred (U.S. 6,289,367).

Re claim 1, Allred discloses in Figure 4 a system for estimating a logarithm of a number (abstract), the system comprising: an integer module (e.g. output of 104 and col. 5 lines 10-20) for determining an integer part of a logarithm of a number (e.g. i or 2^n), a linear approximation module (e.g. 106, 108, and col. 16 lines 35-40) for determining a linear approximation of a fractional part of the logarithm of the number (col. 7 lines 30-35), and an implementation module (e.g. 106 and 108 in Figure 4) for implementing the linear approximation in a single polynomial function for estimating the fractional part; wherein the single polynomial function is used for a range of input values (e.g. equation 24 in col. 10).

Re claim 2, Allred further discloses in Figure 4 the single polynomial function is a second order polynomial (e.g. equation 24 wherein $\{a_0,a_1\} = \{0,0.585x2^{-n+1}xr\}$).

Re claim 3, it is a method claim of claim 1. Thus, claim 3 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 4, it is a method claim of claim 2. Thus, claim 4 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 5, Allred discloses in Figure 4 a circuit for generating an integer part (e.g. output of 104) and an estimate of a fractional part of a logarithm (e.g. 106 and 108), the circuit comprising: a shift register (e.g. 108) for loading a valid input data and for generating an estimate of a fractional part (output of 108); and a counter (e.g. n from 104) for loading a total number of bits in an input data (e.g. col. 6 tables 1 and 2) and for generating an integer part (e.g. n); wherein the circuit implements a single polynomial for generating an improved estimate of the fractional part (e.g. equation 24 in col. 10).

Re claim 6, Allred further discloses in Figure 4 the shift register left shifts data by one bit when a most significant bit of the shift register is substantially equal to zeros (e.g. in case when n=0 then shift by one bit) wherein the shift register left shifts until the most significant bit equals one (e.g. by –n+1).

Re claim 7, Allred further discloses in Figure 4 the counter decrements by one when a most significant bit of the shift register is substantially equal to zero (e.g. in case when n=0 then shift by one bit), wherein the counter decrements until the most significant bit equals one (e.g. by –n+1).

Re claim 8, it is a method claim of claim 5. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 9, it is a method claim of claim 6. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 10, it is a method claim of claim 7. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 11, Allred discloses in Figure 4 a digital circuit for implementing a polynomial for estimating a fractional part of a logarithm of a number (abstract), the circuit comprising: a function circuit (e.g. 106 and 108) for receiving an estimate of a fractional part (e.g. output of 108) and for generating a function of the estimate, wherein the function corresponds to an order of the polynomial (e.g. equation 24 wherein $\{a_0,a_1\}$ = $\{0,0.585x2^{-n+1}xr\}$); a first constant multiplier (e.g. 106) for multiplying the estimate of a fractional part and a second polynomial coefficient and for generating a first output; a second constant multiplier (e.g. 108 by shifting) for multiplying the function of the estimate and a third polynomial coefficient and for generating a second output; a first adder (e.g. equation 42 an adder for subtracting 1) for adding the first output of the first constant multiplier and the second output of the second constant multiplier and for generating a first sum; and a second adder (e.q. 110) for adding the first sum and a first polynomial coefficient and for generating an improved estimate of the fractional part.

Re claim 12, Allred further discloses in Figure 4 the order of the polynomial is two (e.g. equation 42 wherein $\{a_0,a_1\} = \{-1,s_{const}x2^{-n+1}xr\}$).

Re claim 13, Allred further discloses in Figure 4 the function circuit is a squaring circuit (e.g. 108 by left shifting 1 bit).

Re claim 15, it is a method claim of claim 11. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 16, it is a method claim of claim 12. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 17, it is a method claim of claim 13. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 19, Allred discloses in Figure 4 method for estimating a logarithm of a number (abstract), the method comprising the steps of: determining an integer part (e.g. output of 104) of a logarithm of a number, determining (e.g. output of 108) a linear approximation of a fractional part of the logarithm of the number; wherein the linear approximation comprises a fraction minus a constant one wherein a numerator of the fraction is a variable and a denominator of the fraction is two to a power of the integer part (e.g. equation 42 in col. 22); raising the linear approximation to a predetermined power (e.g. 2^{-n+1}), for generating a fraction estimate; multiplying the fraction estimate by a variable (e.g. s_{const}), for generating a product; and summing the product (e.g. equation 42 in col. 22) over a predetermined range for generating a polynomial approximation of the fractional part (output of 108).

Re claim 20, Allred further discloses in Figure 4 the steps are performed to calculate one or more of signal to noise ratio, bit error rate, and power in dB (e.g. col. 3 lines 55-65).

Re claim 21, it has same limitation cited in claim 20. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

Re claim 22, it has same limitation cited in claim 20. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

Re claim 23, it has same limitation cited in claim 20. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 24-29 are rejected under 35 U.S.C. 103(a) as being obvious over Allred (U.S. 6,289,367) in view of admitted prior art.

Re claims 24-25, Allred does not disclose in Figure 4 the system is applied to one or more of ADSL, DSL, and G.SHDSL applications and the system is applied to one or more of central office, customer premise equipment, and wireless applications. However, the admitted prior art disclose in the background of the present invention the logarithm of base 2 system is traditionally applied to ADSL, DSL, G.SHDSL applications for determined power back off (page 2 lines 5-10 and 19-26) through CO and CPE (page 2 lines 3-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to applied the logarithm base-2 computation into the ADSL, DSL, and G.SHDSL applications and the system is applied to one or more of central office, customer premise equipment, and wireless applications as seen in the

admitted prior art's invention into Allred's invention because it would enable to enhance the system by determine specific power back off fast and accurately.

Re claim 26, it has same limitation cited in claim 24. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 27, it has same limitation cited in claim 25. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Re claim 28, it has same limitation cited in claim 24. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 29, it has same limitation cited in claim 25. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Allowable Subject Matter

5. Claims 14 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,365,465 to Larson discloses a floating point to logarithm converter.

b. U.S. Patent No. 5,831,878 to Ishida discloses an exponential and logarithmic conversion circuit.

c. U.S. Patent No. 5,685,008 to Pan et al. disclose a computer processor utilizing logarithmic conversion and method of use thereof.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

January 18, 2005

ANIL KHATRI
PRIMARY EXAMINER